For example, referring to FIGS. 2-4 of the application, the chip carrier includes: a core layer 11 with a plurality of conductive traces 12, at least one first trace 20 connected with a passive component 40 and a having a first predetermined position 22 (see FIG. 2), at least one second trace 30 not connected with the passive component 40 and having a second predetermined position 32 (see FIG. 2), and a solder mask layer 14 exposing the first and second predetermined positions 22 and 32.

As claimed, the first predetermined position 22 and the second predetermined position 32 are formed on the same surface of the chip carrier, i.e., on the top surface of the substrate 10 (see FIGS. 2-4). Also, a first ball pad 27 and a second ball pad 37 are formed on an **opposite** surface of the chip carrier, i.e., on the bottom surface of the substrate 10 (see FIGS. 2-4).

The above-described arrangement allows the first and second ball pads on the same surface to serve as test points contacted by test heads to perform an electrical performance test, and prevents the test heads from contacting bond fingers of a chip carrier during the test, thereby assuring quality and yield of the chip carrier. Also, the Applicants' claimed chip carrier is suitable for use with many devices without modifying the structure or design of the chip carrier.

Claim 1 was rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,646,349 to Pu et al. ("Pu"). Claims 2-7 were rejected under 35 USC 103(a) as being unpatentable over Pu in view of U.S. Patent 6,577,490 to Ogawa et al. ("Ogawa"). Claims 8 and 11-17 were rejected under 35 USC 103(a) as being unpatentable over Pu in view of "Admitted Prior Art" (APA). Claims 9 and 10 were rejected under 35 USC 103(a) as being unpatentable over Pu in view of U.S. Patent 5,698,895 to Pedersen et al. These rejections are respectfully traversed.

It should be noted that Pu is **not** prior art to the subject application under 35 USC 103.

Specifically, Pu does not qualify as prior art under 35 USC 103(c), and therefore cannot be used in a rejection of claims under 35 USC 102(e)/103. The subject application and Pu have

the same assignee, *Siliconware Precision Industries Co, Ltd.* of Taiwan, R.O.C., and were commonly owned at the time the invention was made.

That is, the subject application and Pu were, at the time the invention was made, owned by Siliconware Precision Industries Co., Ltd. Therefore, under MPEP 706.02(l)(2), Pu is not prior art to the subject application under 35 USC 103(c).

Because Pu is not prior art to the subject application for the purpose of obviousness, the rejections under 35 USC 103(a) involving Pu are rendered moot.

Thus, the only remaining rejection is the rejection of claim 1 as being anticipated by Pu.

Regarding the rejection of claim 1, the Pu reference does not teach or suggest a chip carrier in which the positions of first and second traces are located on the same side of a substrate, i.e., where a "first predetermined position" of at least one first trace is located on the same surface as a "second predetermined position" of at least one second trace, and in which first and second ball pads are formed on "an opposite surface of the chip carrier" (claim 1).

Referring to FIGS. 5A and 7A of Pu, as cited in the Office Action, a semiconductor package includes a substrate 10 having a plurality of first conductive traces 11 formed on an upper surface 100 of the substrate 10, and a plurality of second conductive traces 12 formed on a lower surface 101 of the substrate 10 (see column 4, lines 37-44; see also FIG. 1). The lower surface 101 of the substrate 10 also is formed with discontinuities 121 and discontinuous pads 122 (see FIG. 7A).

In Pu, the first conductive traces 11 and the second conductive traces 12 are formed on **different** sides of the substrate 10. However, claim 1 requires the first/second predetermined positions of the first/second traces to be located on the same surface of a chip carrier.

Also, in Pu, the discontinuities 121 are formed on the same surface as the second conductive traces 12 (see, e.g., FIG. 1 of Pu). However, claim 1 requires the first and second ball pads to be formed on an opposite surface relative to the first/second predetermined positions of the first/second traces.

For at least the reasons discussed above, the Pu reference does not anticipate or otherwise render obvious the Applicants' claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

Date: March 31, 2006

Peter F. Corless (Reg. No. 33,860)
Steven M. Jensen (Reg. No. 42,693)
EDWARDS & ANGELL, LLP
P.O. Box 55874
Boston, MA 02205

Phone: (617) 439-4444

Customer No. 21874